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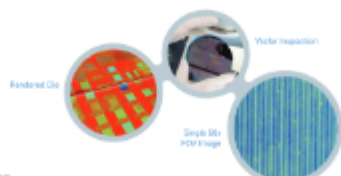
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### Full-Field Hotspot Detection and High-Resolution Topographic Characterization of Post-CMP Wafers with 3D Optical Profiling

Traditional methods of post-CMP process evaluation have analytical limitations that, in light of tightening process control limits, do not meet the growing need for more accurate wafer surface characterization in semiconductor chip manufacturing. This application note describes how white light interferometry (WLI) enables advanced packaging manufacturers and CMP specialists to obtain critical data from the high-resolution, full-die maps this 3D optical profiling technique makes possible.

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Application Note #576

#### Full-Field Hotspot Detection and High-Resolution Topographic Characterization of Post-CMP Wafers with 3D Optical Profiling

For decades, chemical mechanical polishing (CMP) or planarization has been the predominant technique for smoothing and flattening wafer surfaces during semiconductor integrated chip (IC) fabrication. Post-CMP evaluation is now standard practice for ensuring adequate planarity of the IC layers and conforming compliance with planarity requirements. However, traditional methods of post-CMP process evaluation have analytical limitations that, in light of tightening process control limits, have given rise to a growing need for more accurate wafer surface characterization in semiconductor chip manufacturing. Post-CMP assessment with advanced 3D optical probe technology presents an optimal alternative, enabling both more accurate and more timely identification of CMP integration issues, thereby reducing the manufacturing costs of meeting the demands of contemporary IC design trends. This application note describes the use of white light interferometry (WLI) for post-CMP wafer characterization, and how advanced packaging manufacturers and CMP specialists can obtain critical data from high-resolution, full-die maps this 3D optical profiling technique makes possible.

#### Methodology Considerations for CMP

Semiconductor chip manufacturers use CMP both to remove excess dielectric and metal materials after deposition and between layers to provide adequate

surface planarity for the next process step. CMP has become one of the most critical processes involved in chip manufacturing due to the continuous miniaturization of IC technologies. Other recent industry innovations in 3D memory stacking technology (e.g., 3D NAND memory), heterogeneous integration (e.g., CoWoS), and advanced packaging have also imposed additional constraints on CMP specifications and increasingly have tightened CMP process requirements.

Manufacturers and CMP professionals often collect localized, small-area surface topography measurements to assess CMP process performance for both IC and reticle inspection. However, because variation in pattern density and size across the die can cause non-uniform planarization, such small-area measurements may not be representative of the full-die CMP topography. With high vertical resolution, high throughput, and axial invariance capabilities, Bruker's WLI-based 3D optical profilers overcome this analytical limitation, easily and quickly collecting large-area surface topography measurements level-to-level, and delivering full-die maps with angstrom-level vertical resolution and micron-level lateral resolution to provide more reliable assessment of wafer surface planarity and CMP process efficacy.

#### Full-Die Map via Image Stitching

The use of stitching of traditional post-CMP wafer characterization derive from the inability to collect data



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